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Tutorial Microelectronics III

WS 2019/20

1. Devices in MOS-Technology

Task 1:

Calculation of Capacity of Interconnects and of Square Resistance

The minimum width and the capacity of metal-connection in 0.25 µm CMOS technology is listed in Figure 1.

	Metal1	Metal2	Metal3	Metal4
Minimum Width (µm)	0.25	0.35	0.45	0.50
Area Capacity (aF/µm$_2$)	30	15	9	7
Perimeter − Capacity (aF/µm)	80	50	40	30

Figure 1: Minimum Width and Capacities of Interconnects

a) An interconnect with length *1000µm* and width *1µm* is necessary in a circuit. The *square resistance* of Metal 1 to 3 is *80mΩ/□* and of Metal 4 *40mΩ/□*. With which Metal-Interconnect the time delay is minimal?

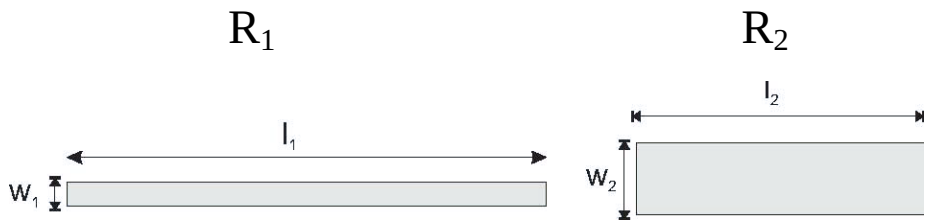

Figure 1: Layout of Resistors

b) Determine the nominal-resistance value R_1 and R_2. The sheet resistance is *30Ω/□*, l_1 *=20 µm*, w_1 *=1 µm*, l_2 *=12 µm* and w_2 *=3 µm*.

c) The process variation (mask misalignment) is now 0.1 *µm*. Please determine the range of resistance ratio R1/R2 due to this inaccuracy.

d) How high is the fault if the design parameter (l and w) are doubled? And what is the disadvantage?

e) Please use a layout method to minimize the fault?